Rapid Thermal Processing of α-Hexathienylene Thin-Film Transistors

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In this paper we show that rapid thermal annealing of as-deposited p-type α-hexathienylene (α-6T) thin-film transistors (TFTs) can yield devices with *on/off* current ratios higher than 10^6. Such high *on/off* ratios, together with switching times of ~10 μs and compatibility of the active material with flexible plastic substrates, render α-6T TFTs potential candidates as switching devices in plastic-substrate-based active-matrix displays. We also report on the morphological, structural, and electrical characteristics of α-6T films and TFTs when subjected to rapid thermal heating above the melting point of α-6T.

Introduction

Semiconducting materials that can be deposited and processed at temperatures compatible with a plastic substrate are being actively investigated for the fabrication of low-cost, robust, and flexible plastic displays. Thin films composed of small organic molecules or polymers are suited for these requirements and are therefore being increasingly studied and employed as active layers in light-emitting diodes and all-organic thin-film transistors (TFTs).[1,2]

α-Hexathienylene (α-6T) and other thiophene oligomers show very promising TFT performance, particularly when they are synthesized and purified by the procedures proposed by Katz *et al.*[3] These procedures result in purer materials with much reduced impurity levels.[3] Careful attention to device design[4] using materials synthesized as above has resulted in the demonstration of α-6T TFTs with mobilities of 0.01–0.08 $cm^2/(V\ s)$ and switching times of about 10 μs.[4] When ultrapure α-6T is employed, TFTs with *on/off* ratio in excess of 10^6 can be obtained.[3] These figures of merit represent a definite improvement with respect to the previously published results. The utility of α-6T TFTs in displays will be further enhanced if mobilities ≥0.1 cm^2/V s can be obtained.

α-6T films deposited by sublimation on substrates held at room temperature exhibit a grainlike morphology. These grains have typical dimensions of 0.1 μm and a crystalline structure with α-6T chains oriented nearly normal to the substrate.[5] The residual conductivity is p-type (the typical carrier concentration is about 10^{17} cm^{-3}) and arises from adventitious dopants which might be either impurities or lattice defects. The apparent field-effect mobility (μ) in α-6T TFTs is electric-field dependent; μ becomes larger when the applied electric field between source and drain contacts in the channel region is higher than 10^5 V/cm.[6] The field dependence of the apparent mobility was deduced from the analysis of the current–voltage (I–V) characteristics of α-6T TFTs with different channel lengths using the analytical model that we developed for organic TFTs.[6] In fact, from an analysis of the I–V characteristics of α-6T TFTs with channel length L = 1 μm, we measured a mobility as high as 0.08 cm^2/V s.[7] Field-dependent mobilities have already been observed in other insulating and semiinsulating polymers.[8,9]

TFTs used as switching devices in active-matrix displays must have an *on/off* ratio ≥10^6 and operate in the enhancement mode. In this paper we report a procedure that transforms enhancement/depletion-mode-operating α-6T TFTs with poor *on/off* ratios into devices with ratios in excess of 10^6 operating only in the enhancement mode. We also report on the morphological, structural, and electrical modification of α-6T films and TFTs when subjected to rapid thermal processing (RTP) beyond the α-6T melting point. Furthermore, in order to evaluate the role of the organic/dielectric interface, the RTP study has been extended to α-6T films deposited not only on amorphous substrates such as SiO_2 but also on single-crystal substrates such as (100) Si and randomly sectioned single-crystal sapphire.

Experimental Section

α-6T has been synthesized and purified using the procedure developed by Katz et al.;[3] the melting point of this purified form of α-6T is 313.5 °C in an inert atmosphere.[3] The concentration of adventitious dopants in such a material depends upon the extent of purification. For this work we *do not* employ the ultrapure α-6T reported in ref 3, and therefore the films are p-type. Films of α-6T were prepared by subliming the material

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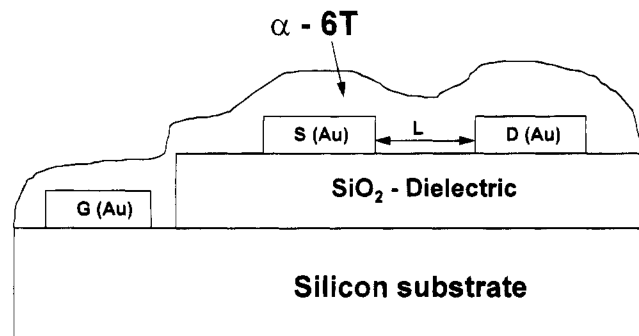

Figure 1. Schematic structure of an α-6T TFT.

onto the substrate under a vacuum of about 10^{-6} Torr. The deposition rate was 0.5−1 nm/s and the substrate temperature was in the 20−25 °C range. Film thicknesses, over which we have a ±2.5 nm control, were varied from 50 to 200 nm.

α-6T films were also deposited on single-crystal substrates such as Si (100) and randomly sectioned single-crystal sapphire. All the substrates had been carefully cleaned in organic solvents and deionized water using an ultrasonic bath, and then spun dry. Additionally, the silicon substrates were further cleaned using the RCA procedure,[10] and the native oxide was subsequently etched in HF/deionized water 1:10 for 10 s, after which the wafer was spun dry. This procedure is said to prevent the regrowth of the native oxide for several hours.[11]

Rapid thermal processing (RTP) was conducted on α-6T films deposited on all the substrates previously described using an AG Associates Heatpulse 410 annealing system in a nitrogen atmosphere. The temperature was increased and lowered at a nominal rate of 100 °C/s and the samples were heated for about 1 s at the highest temperature. The measured temperature is accurate to within ±1 °C.

Atomic force microscopy was performed with a commercial instrument (Park Scientific) using a SiN pyramidal tip in the contact mode. Scanning electron microscopy was performed in a JEOL JSM 840 on α-6T/SiO_2 samples that had been sputtered with gold.

X-ray diffractograms of films on the different substrates were obtained in the reflection mode at 40 kV and 25 mA using scanning rates of 0.5−1.0° 2θ/min and Ni-filtered Cu Kα radiation from a 2-kW Rigaku X-ray generator.

The TFTs were fabricated on thermally oxidized Si substrates. The thickness of the oxide was d = 300 nm (capacitance per unit area C_i = 10 nF/cm^2) and the resistivity of the Si was 5−10 Ω cm. The Si substrate with a gold ohmic contact functions as the gate and the oxide as the gate dielectric. Gold source and drain contacts were photolithographically defined on the SiO_2 such that Z = 250 μm was the gate width and L = 1.5, 4, 12, and 25 μm were the channel lengths. The TFT structure is shown in Figure 1. Transistor characteristics (source current, I_D, vs source-drain voltage, V_D) were measured with a Hewlett-Packard 4145B semiconductor parameter analyzer at different gate voltages (V_G) at room temperature and under vacuum. With zero gate bias, the TFT has a low p-type conductivity, which scales with the thickness of the organic layer. In such TFTs, a hole current is measured if the source is biased negatively with respect to the drain. This is due to the charges already present in the unintentionally p-doped film. When a positive gate bias is applied, the channel conductivity is lowered and the device operates in the depletion mode until the *off*-current limit is reached. Consequently the threshold voltage (V_T) in this device is positive in sign and marks the passage from *off* to *on* conductivity of the channel during depletion-mode operation ($V_G \geq 0$). When the gate bias (with respect to the source) is negative, an accumulation layer is formed at the α-6T/SiO_2 interface which increases the conductivity of the channel, and the device operates in the enhancement mode. In the following, we will refer to the *on*/*off* ratio of the TFT as at the ratio between I_D currents at $V_G = -100$ V and at $V_G = 0$ V measured at a certain V_D in the saturation regime.

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Results and Discussion

Rapid thermal annealing (RTA) of α-6T TFTs at temperatures between 250 and 310 °C for 1 s causes a distinct enhancement of the size of the grains that constitute the organic film. This can be seen from the atomic-force micrographs (AFMs) of α-6T TFTs annealed at different nominal temperatures (Figure 2). The AFM of the as-deposited α-6T film demonstrates average grain sizes of about 0.1 μm (Figure 2a). When these samples are annealed at 30−60 °C below the melting point of α-6T, the grains become as large as 0.3−0.5 μm (Figure 2b); they reach the micron scale (Figure 2c) when the rapid thermal annealing is carried out at temperature close to the melting point (i.e., at 290−310 °C). Figure 2c also shows that the grains remain in physical and electrical contact despite the mass movement accompanying their growth during annealing. However, surprisingly, the rapid thermal annealing modifies the $I-V$ characteristics of α-6T TFTs. In Figure 3 a comparison between the electrical characteristics of annealed and as grown α-6T TFT is presented. These data are all from L = 25 μm transistors. The as-deposited α-6T TFT shows a clear depletion-mode operation with a threshold voltage, V_T, as high as 40 V (Figure 3a). Because of the fact that α-6T is not an intrinsic semiconductor and the film is 150 nm thick, the *on*/*off* ratio is as low as 90. When the transistor is annealed at about 30−60 °C below the melting point (Figure 3b) we found that the threshold voltage is lowered (V_T = 20 V) and the *on*/*off* ratio increases to a maximum of 2×10^3 (an average value of 4×10^2 is measured). When the rapid thermal annealing is performed at a temperature very close to the melting point and the grains become as large as 1−3 μm without losing physical and electrical continuity, the $I-V$ characteristics change as shown in Figure 3c. The threshold voltage is zero, i.e., no more depletion-mode operation occurs, and the *on*/*off* ratio is $>10^6$ if the probe leakage (~30 pA) is factored out. The average measured *on*/*off* ratio is 8×10^4. The discrepancy between the best and the average values of the *on*/*off* ratio is attributed to nonuniform heating during the very rapid annealing treatment. Despite the scatter, the trend of increasing *on*/*off* ratio with annealing temperature is clear. $I-V$ characteristics have also been measured for TFTs with channel lengths of 12 and 4

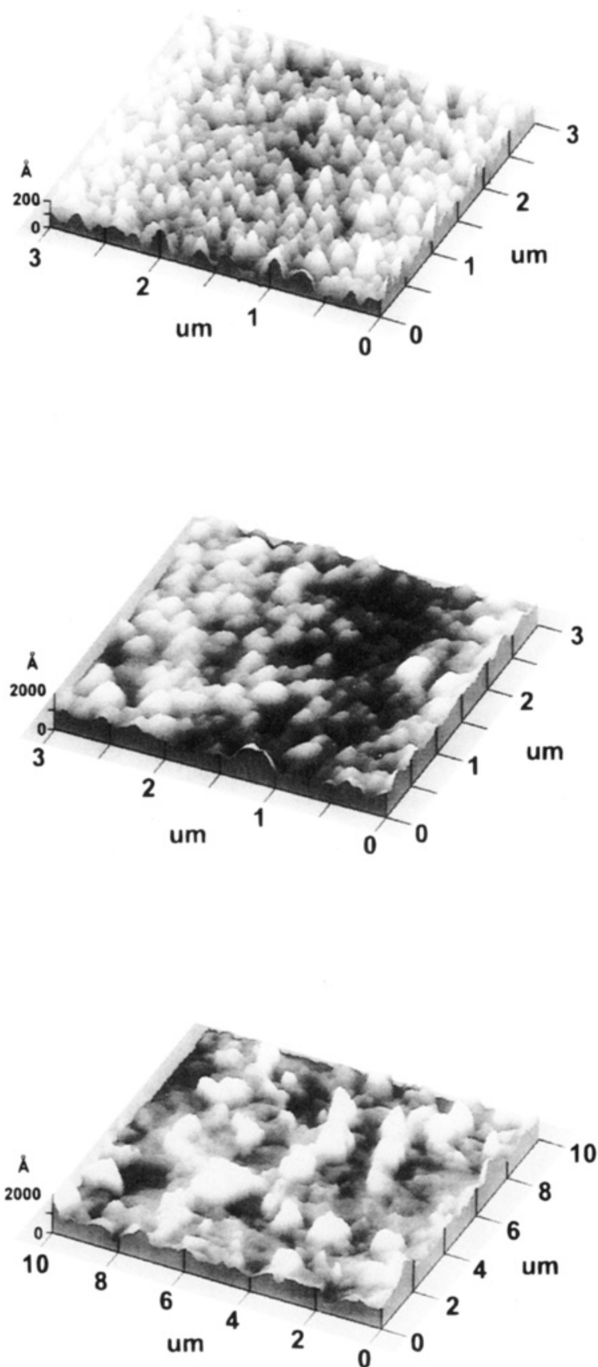

Figure 2. Atomic force micrographs of (a) an α-6T TFT as grown on a Si/SiO_2 substrate, (b) after rapid thermal annealing at 274 °C, and (c) after rapid thermal annealing at 304 °C. The initial thickness of the α-6T films were 150 nm.

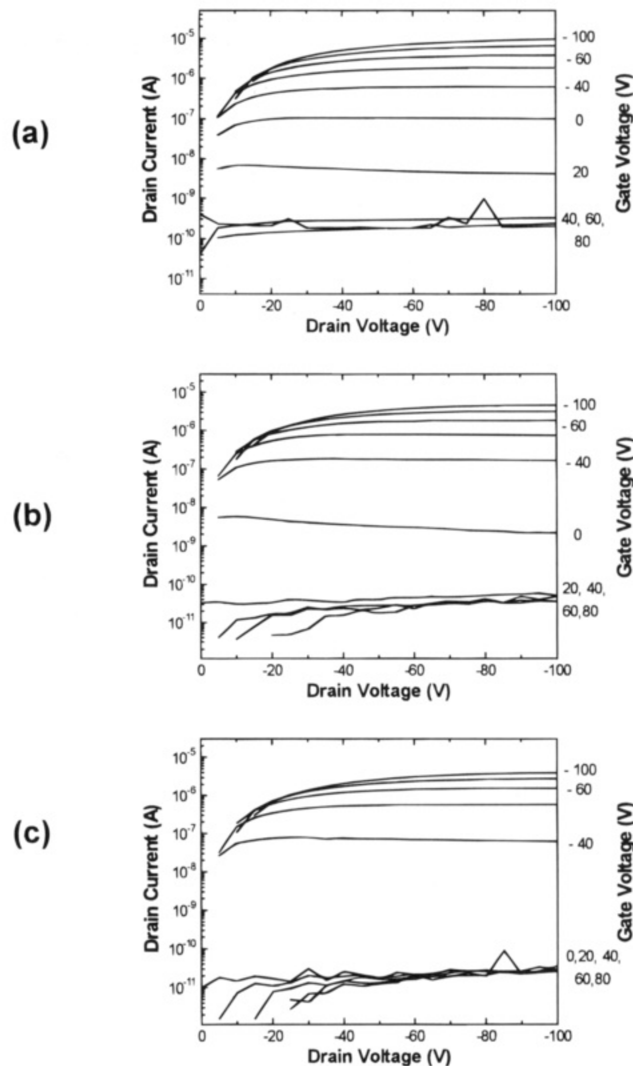

Figure 3. Current–voltage characteristics for α-6T TFTs (L = 25 μm, W = 250 μm, film thickness = 150 nm) (a) before annealing, (b) after annealing at 274 °C, and (c) after annealing at 304 °C.

Table 1. *On/off* Current Ratios of α-6T TFTs (Ratio of Drain Currents at $V_G = -100$ and $V_G = 0$ V) with Different Channel Lengths Using α-6T As-Deposited and after Different Annealing Treatments

	on/off current ratios				
TFT channel length, μm	as-deposited	annealed at 274 °C		annealed at 304 °C	
25	90	max 2×10^3	av 4×10^2	max $>10^6$	av 8×10^4
12	50	125		max 3.5×10^3	av 6×10^2
4	50	100		2×10^2	

μm. The corresponding *on/off* ratio values are reported in Table 1. In these cases the increase of the *on/off* ratios with annealing temperature is also clearly evident. This ratio is seen to decrease when the channel length becomes shorter; this is expected from the corresponding increase in *off* current,[6] as is observed in many other systems. The lowering of the transistor *off* current upon annealing may be a result of the reduction in the number of defects or of electrically active impurities in the organic film. Rapid thermal annealing can cause both desorption of volatile impurities and reduction in the number of lattice defects. However the field-effect mobility of TFTs does not improve after the transistor is annealed, even when the macroscopic grain size exceeds the channel length. A possible explanation for this observation is given below.

The morphology of the α-6T film changes completely when the rapid thermal processing (RTP) is carried out at a temperature higher than the melting point of α-6T. A scanning electron micrograph (SEM) of an α-6T film recrystallized from the melt is shown in Figure 4a. This α-6T film was deposited on SiO_2 whose surface had been previously cleaned by etching in HF/deionized H_2O (1:10) for 10 s. The film appears regularly crystalline, and the AFM images reveal that the surface is no longer granular but is smooth and compact on the submicron scale. Optical microscopy shows that crystals as large

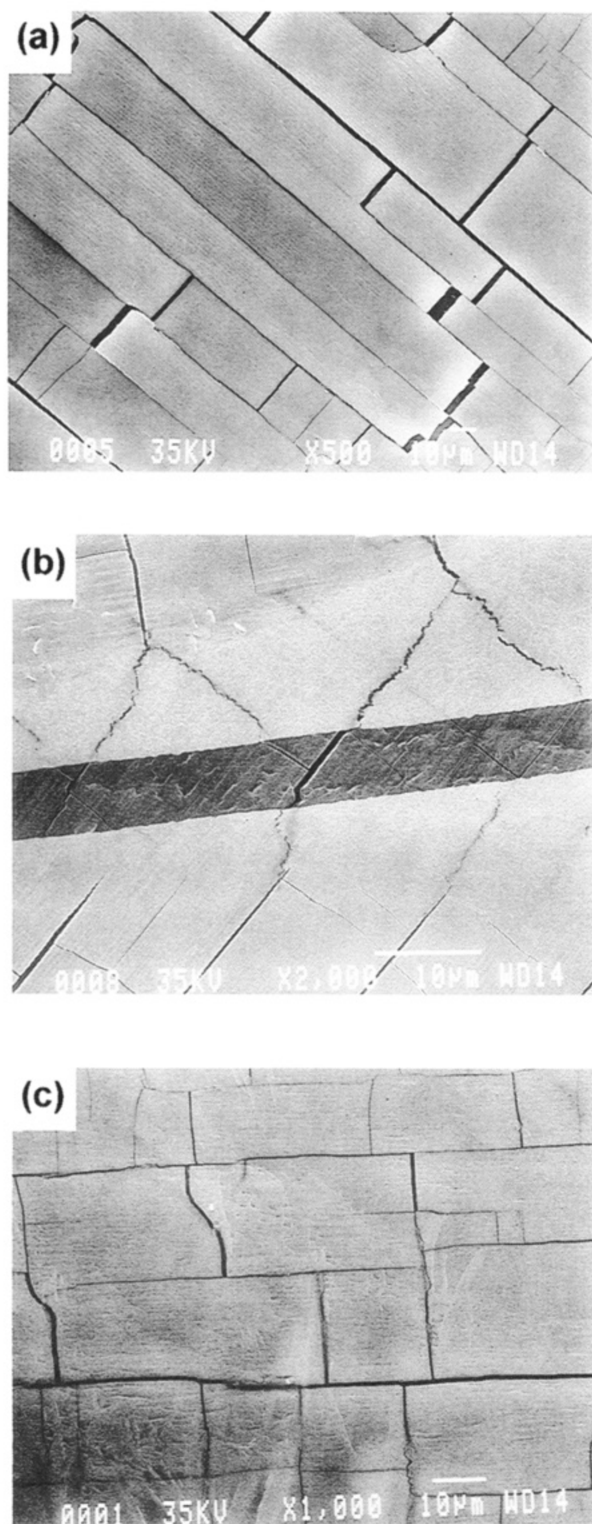

Figure 4. Scanning electron micrographs of α-6T films deposited on different substrates and subsequently heated for 1 s above the melting point of α-6T. (a) α-6T film on an unpatterned SiO_2 substrate; (b) α-6T film on a Si/SiO_2 TFT substrate (detail of source and drain gold pads separated by a 4 μm channel); (c) α-6T film on a Si substrate treated as described in the text.

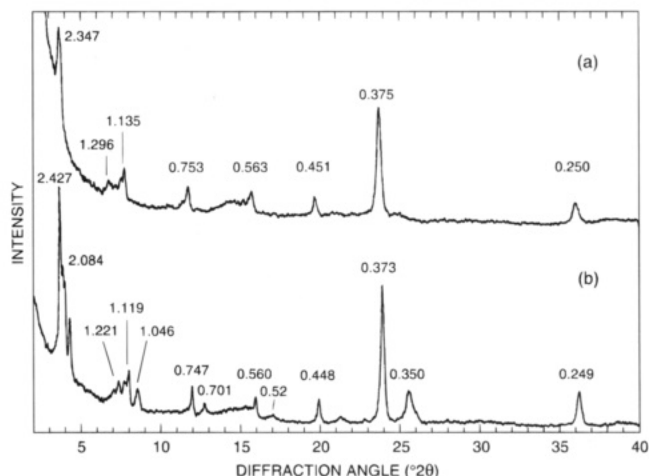

Figure 5. X-ray diffractograms (reflection mode) of α-6T films deposied on (a) SiO_2 and (b) Si substrates and subsequently heated for 1 s above the melting point of α-6T. The Si substrate has been treated as described in the text.

as 100 μm × 20 μm can be created. These crystals show a variety of orientations, demonstrating lack of epitaxial growth. Clearly, the most striking features introduced by recrystallization from the melt are the extensive internal fractures seen in Figure 4a. A separate study of single-crystal growth and characterization using electron diffraction[12] showed that the long axis of the crystals corresponds to the (204)* and the short one to b^*; this indicates[12] that the fractures occurs between the densely packed (204) planes (here the nomenclature is that from the single-crystal structure analysis of Siegrist et al.[13]). Careful inspection of Figure 4a also shows that the corners of the crystals are detached from the substrate; this could be a consequence of poor adhesion between the annealed film and the SiO_2 surface.

In Figure 4b a scanning micrograph of the active region (source and drain pads separated by a 4 μm channel) of an α-6T TFT sample heated beyond the melting point is shown. The crystals of α-6T are large enough to cross the channel and to allow the measurements of their $I-V$ characteristics. Crystals of α-6T can also exhibit the same morphologies when grown on a carefully cleaned (100) Si substrate after melting of a sublimed α-6T film (Figure 4c).

The X-ray diffractograms of α-6T films that had been deposited on SiO_2 or Si and then momentarily heated beyond the melting point are seen, respectively, in Figure 5. The patterns are dominated by reflections of the end-on orientation of α-6T chains, i.e., the molecular repeat in the 2.2–2.4 nm range and its monomeric counterpart at 1/6 of the spacing (i.e., about 0.38 nm). Intermediate orders of the same series are also seen, corresponding to $^1/_2$, $^1/_3$, and $^1/_4$ of the chain repeat. On the contrary, the dominant peaks elicited previously in the 0.44–0.47 nm region from *solution*-precipitated specimens[5] are now only weakly present. These peaks arise[5] from crystallographic planes *containing* the molecules, and thus their weak appearance confirms our inference that the molecules are arranged more or less end-on on the substrate.

The sample on clean Si (Figure 5b) shows an interesting additional feature, namely the existence of a second ordered set of peaks at ca. 0.35, 0.52, 0.70, 1.04, and 2.08 nm. We have recently shown[13] that this set is also attributable to end-on molecular arrangements but for

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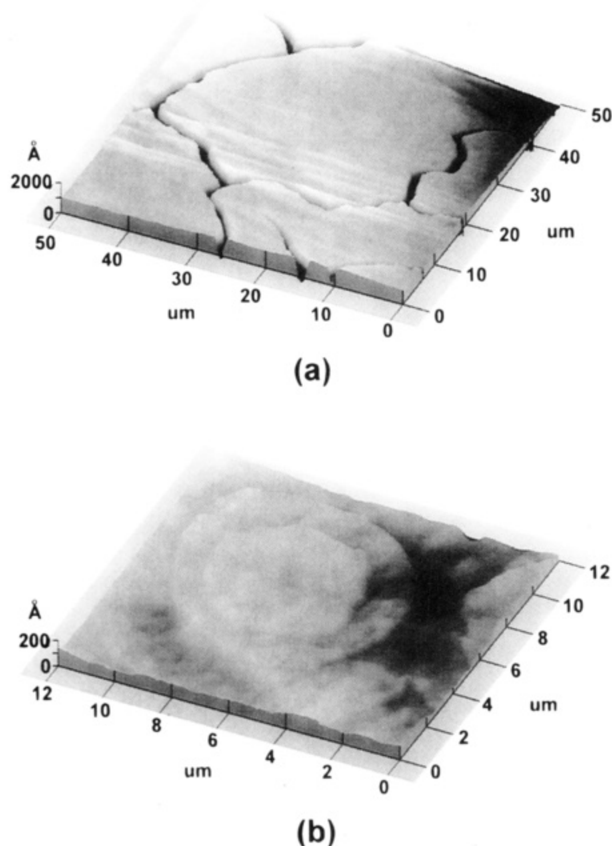

Figure 6. Atomic force micrographs of an α-6T film deposited on a substrate of single-crystal sapphire randomly sectioned and subsequently heated for 1 s beyond the melting point of α-6T.

a *second* polymorph that grows preferentially from the melt at high temperatures. We attribute this difference to possible higher superheating or slightly less rapid cooling for the specimen of Figure 5b, thus shifting the balance slightly toward the high-temperature form.

Interesting features can also be observed in the morphology of α-6T films deposited on randomly sectioned single-crystal sapphire. The sample is once again subjected to rapid heating beyond the melting point of α-6T for 1s. In Figure 6a, the AFM topographic image of this sample is shown. In this case as well, fractures of a few microns are seen to traverse irregularly through the large, flat crystals. No regular crystallographic faceting is observed although there are suggestions of microfaceting on the submicron scale. The fracture on any of the substrates examined implies very different thermal expansion coefficients between α-6T and them, but the irregularity of the cleavage features here may reflect better adhesion with sapphire, perhaps because of its more polar nature.

Details at higher magnification (Figure 6b) include formation of terraces, which, once again, display no regular crystallographic faceting. Interestingly, the step height is equivalent to one monolayer of α-6T (about 2.5 nm[4]). This result is also consistent with our X-ray diffractograms which show that the α-6T chains are, as before, preferentially oriented nearly normal to the substrate.

Surprisingly, the field-effect mobility of α-6T TFTs does not improve after rapid thermal annealing, even though the grains grow to sizes approaching the device channel length; μ becomes even worse when the sample is heated beyond the melting point of α-6T. In fact the $I-V$ characteristics from devices such as that of Figure 4b are poor and in some cases indicate extremely low or zero conductivity. One possible explanation for this behavior is that after the recrystallization of α-6T from the melt, the induction of the charge at the interface between SiO_2 and α-6T could be inhibited because of the poor adhesion of the crystalline organic film to the dielectric. Additionally, as we showed in Figure 4, the thermal stresses cause extensive fractures in the crystalline film; fine fractures have been demonstrated to occur even on the submicron scale within single crystals of α-6T by high-resolution electron[5] and atomic force microscopies.[12] This experimental evidence could explain why the very large crystals of α-6T that we grew by rapid thermal processing above the melting point did not result in any improvement in mobility. Extension of our study to other α-6T/gate dielectric systems in an effort to improve adhesion, minimize intracrystalline fracture, and perhaps achieve higher mobilities, will be described in a future report.

Conclusions

We have demonstrated that rapid thermal annealing of TFTs with p-type α-6T active layers leads to substantial enhancement in *on/off* current ratios. This increase of the on/off ratio is due not to enhanced mobility but rather to decreased *off* current. When these TFTs are subjected to rapid heating beyond the melting point of α-6T, crystals with lateral dimensions $>10\ \mu m$ can be grown from the melt. After such thermal processing, the α-6T chains continue to be oriented nearly normal to their substrates; this has been verified for a number of substrates, including SiO_2, oxide-free Si (100) and single-crystal sapphire. The surface morphology, faceting, and fracture patterns of α-6T were found to depend on the substrate.

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